AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A memory device for a mobile phone comprising:

a flash memory for storing program data and user data;

an interface circuit for copying program data stored in the flash memory according to whether data stored in the flash memory is valid;

a first ~~memory~~ Random Access Memory (RAM) for providing an operation area to store and execute the copied program data; and

a second ~~memory~~ RAM for storing data generated during the execution of program data,

wherein the first and second ~~memories~~ RAMs are independent memories.

2. (Original) A memory device as in claim 1, wherein the flash memory is a NAND-type flash memory.

3. (Original) A memory device as in claim 1, wherein the first and second memories are random-access memories (RAM).

4. (Original) A memory device as claimed in claim 1, wherein the interface circuit is an application-specific integrated circuit (ASIC) including a read-only memory (ROM) for storing program codes and an error correction circuit.

5. (Original) A memory device as in claim 1, wherein the interface circuit comprises a

first logic gate for generating a NAND CE (chip enable) signal, said NAND CE signal enabling the flash memory.

6. (Original) A memory device as in claim 5, wherein the interface circuit further comprises a second logic gate for generating a CLE (command latch enable) signal, said CLE signal informing the flash memory that incoming data is a command.

7. (Original) A memory device as in claim 6, wherein the interface circuit further comprises a third logic gate for generating a ALE (address latch enable) signal, said ALE signal informing the flash memory that incoming data is an address.

8. (Original) A memory device as in claim 5, wherein the first logic gate is an OR gate for receiving a CS (chip select) signal from the microprocessor and a CE (chip enable) signal from the microprocessor for generating said NAND CE signal.

9. (Original) A memory device as in claim 6, wherein the second logic gate is an AND gate for receiving a command signal from the microprocessor and a CS (chip select) signal from the microprocessor for generating said CLE signal.

10. (Original) A memory device as in claim 7, wherein the third logic gate is an AND gate for receiving an address signal from the microprocessor and a CS (chip select) signal from the microprocessor for generating said ALE signal.

11. (Previously Presented) A mobile communication device comprising:

an analog circuit for air interfacing the mobile communication device;

a user interface circuit for interfacing between the mobile communication device and a user, wherein the interface circuit is an application-specific integrated circuit (ASIC) including a read-only memory (ROM) for storing program codes and an error correction circuit;

a microprocessor (MPU) for providing overall control of the operation of the mobile device; and

a memory device including

a flash memory for storing program data and user data;

an interface circuit for interfacing the flash memory to the microprocessor;

a first memory for copying the program data of the flash memory; and

a second memory for executing the program data of the first memory,

wherein the first and second memories are independent memories.

12. (Original) A mobile communication device as in claim 11, wherein the flash memory is a NAND-type flash memory.

13. (Original) A mobile communication device as in claim 11, wherein the first and second memories are random-access memories (RAM).

14. (Cancelled)

15. (Original) A mobile communication device as in claim 11, wherein the interface

circuit comprises a first logic gate for generating a NAND CE (chip enable) signal, said NAND CE signal enabling the flash memory.

16. (Original) A mobile communication device as in claim 15, wherein the interface circuit further comprises a second logic gate for generating a CLE (command latch enable) signal, said CLE signal informing the flash memory that incoming data is a command.

17. (Original) A mobile communication device as in claim 16, wherein the interface circuit further comprises a third logic gate for generating a ALE (address latch enable) signal, said ALE signal informing the flash memory that incoming data is an address.

18. (Original) A mobile communication device as in claim 15, wherein the first logic gate is an OR gate for receiving a CS (chip select) signal from the microprocessor and a CE (chip enable) signal from the microprocessor for generating said NAND CE signal.

19. (Original) A mobile communication device as in claim 16, wherein the second logic gate is an AND gate for receiving a command signal from the microprocessor and a CS (chip select) signal from the microprocessor for generating said CLE signal.

20. (Original) A mobile communication device as in claim 17, wherein the third logic gate is an AND gate for receiving an address signal from the microprocessor and a CS (chip select) signal from the microprocessor for generating said ALE signal.